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REMARKS

I. CLAIMS 1 AND 3 ARE NOT ANTICIPATED BY NAKANISHI ET AL.

Claims 1 and 3 stand rejected under 35 U.S.C. § 102 over Nakanishi et al. ("Nakanishi"). Claim 1 is independent. This rejection is respectfully traversed for the following reasons.

A. Claim 1

The Examiner maintains that the test pad 3 in Nakanishi is "for testing an electrical connection between the circuit of the chip IP and the wires" as recited in claim 1. The Examiner does so by arguing that the test pad 3 inherently tests "the electrical properties of the circuit in the chip through the wirings" and therefore necessarily tests the electrical connection ***between*** the circuit and wires.

First, it is respectfully submitted that Nakanishi is completely silent as to any testing performed by pad 3, and the Examiner's assumption that the pad 3 MUST test electrical properties of the circuit in the chip1, rather than other possible tests, is improper. It is quite possible that the test pads are simply spare connections used to connect external signals/power lines, or used for some other known function/testing other than specifically testing the electrical properties of the circuit in the chip. The mere fact that the pads are entitled "test" pads by Nakanishi does not necessitate that they are configured to perform the specific test relied on by the Examiner. It is respectfully submitted that the type of testing performed by pad 3, if any, can not be read into the disclosure of Nakanishi. As previously mentioned, "inherency may not be established by probabilities or possibilities", *Scaltech Inc. v. Retec/Tetra*, 178 F.3d 1378 (Fed. Cir. 1999). Accordingly, even assuming *arguendo* the test pad 3 of Nakanishi is "probably"

used to test electrical properties of the circuit in the chip 1, such a determination is not sufficient to render Nakanishi anticipatory under § 102. Moreover, as discussed above, there are other possible functions for the pad 3.

Second, even assuming *arguendo* that the pad 3 is used for testing the electrical properties of the circuit in the chip, it is NOT necessary for the pad 3 to be used to ***test*** the electrical connections ***between*** the chip and wires as alleged by the Examiner. Rather, it is necessary only for there to be a good connection between the chip and wires so that electrical properties of the chip can be communicated through the wires. Having a good connection between the chip and wires is NOT equivalent to ***testing*** the connection between the chip and wires. It is respectfully submitted that even if the pad 3 is used to test the chip, such testing is not tantamount to affirmatively testing the actual connection between the chip and wiring. As is known, chip testing and connection testing can require different elements and arrangements of those elements.

The Examiner states that the features of "test pins" and "quick and easy testing mechanism" are not recited in the rejected claims. However, contrary to the Examiner's assertion, Applicants are NOT relying on these specific features for arguing that Nakanishi does not disclose claim 1. Instead, it is respectfully submitted that these features (e.g., test pins) are examples of elements which can be used for testing the electrical connection between a chip and wiring substrate. Whereas, because Nakanishi does NOT disclose any such features, the pad 3 of Nakanishi does not inherently test "an electrical connection between the circuit of the chip IP and the wires" as recited in claim 1. That is, Nakanishi does not suggest any structure or arrangement of structures which

would ***necessitate*** the pads 3 being used to test the electrical connection between the chip and wirings.

For example, in one embodiment, voltage sources can be applied to two specifically arranged test pads, connected to and from the circuit, via respective test pins (one for applying voltage and one for detecting) so as to measure subsequent current flow between the wires and the circuit (e.g., through a diode as shown in Figure 3A; *see, e.g.,* claim 4). In contrast, Nakanishi discloses only that the test pads 3 serve as an intermediary for signals sent between chips 1,1' (*see, e.g.,* col. 6, lines 31-40). The Examiner has not established that the arrangement and connections of test pads 3 are adequate to perform testing, let alone ***necessarily*** function to perform testing. That is, Nakanishi does not disclose any elements which can be used to support the Examiner's position that Nakanishi MUST operate to test the electrical connection between the chip and wiring substrate.

As anticipation under 35 U.S.C. § 102 requires that each and every element of the claim be disclosed, either expressly or inherently, in a single prior art reference, *Akzo N.V. v. U.S. Int'l Trade Commission*, 808 F.2d 1471 (Fed. Cir. 1986), based on the foregoing, it is submitted that Nakanishi does not anticipate claim 1, nor any claim dependent thereon.

B. Claim 3

Regarding claim 3, the Examiner does not appear to address Applicants' previously filed arguments against the pending rejection. The Examiner is directed to MPEP § 707.07(f) under the heading "Answer All Material Traversed" sets forth the applicable requirement:

> [w]here the applicant traverses any rejection, the examiner should, if he or she repeats the rejection, take note of the applicant's argument and answer the substance of it.

For the examiner's convenience, Applicants' arguments with respect to claim 3 are herein repeated. If the Examiner maintains this rejection, it is respectfully requested that the Examiner respond to said arguments.

Turning to the rejection of claim 3, the Examiner merely alleges that the test pad 3 of Nakanishi "is a portion of the at least one of the wires ... ." However, none of the test pads 3 of Nakanishi appear to be formed of wires in the substrates 17,18 and none of the wires of Nakanishi appear to form part of test pads 3. Rather, Nakanishi appears to disclose only that wires of the substrates are connected to the pads 3.

Based on all the foregoing, it is submitted that claims 1 and 3 are patentable over Nakanishi. Accordingly, it is respectfully requested that the rejection of claims 1 and 3 under 35 U.S.C. § 102 be withdrawn.

II. CLAIMS 4 AND 5 ARE PATENTABLE OVER NAKANISHI ET AL. IN VIEW OF VOLDMAN

Claims 4 and 5 stand rejected under 35 U.S.C. § 103 over Nakanishi in view of Voldman ('280). This rejection is respectfully traversed for the following reasons. Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.,* 819F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as claim 1 is patentable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also patentable. In addition, it is respectfully submitted that the

dependent claims are patentable based on their own merits by adding novel and non-obvious features to the combination recited in claim 1.

With respect to claims 4 and 5, the Examiner maintains the rejection by alleging that a diode connection can be added to Nakanishi for protecting against electrostatic discharge ("ESD") as taught by Voldman. However, as Voldman and Nakanishi appear to be drawn to semiconductor devices which are functionally/structurally remote from one another (voltage regulator bypass and wiring substrate, respectively), the Examiner has not provided any objective evidence that the device of Nakanishi would be subject to ESD. Accordingly, there is no ***disclosed*** need or desire to add a protection diode into the device of Nakanishi. As such, it is respectfully submitted that the Examiner's merely selected bits and pieces of the prior art and relied solely on improper hindsight reasoning using only Applicants' specification as a guide to reconstruct the claimed invention.

Furthermore, it is not disputed that it is known to use diodes for reducing noise generally. However, it is respectfully submitted that the specific connection of a test pad to the ground (or power line) and a node in the circuit, and the incorporation of a diode between the ground (or power line) and node in the circuit, is novel and non-obvious as none of the cited prior art suggests such a ***combination***. According to the present invention as recited in claims 4 and 5, it can be possible to verify the connection between the IP and the wire by measuring the current flowing in the forward direction of the diode during testing. At best, the Examiner has attempted to show only that the elements of the claimed invention are ***individually*** known without providing a *prima facie* showing of obviousness that the ***combination*** of elements recited in the claims is known or suggested

in the art. For all the foregoing reasons, it is submitted that the proposed combination of Nakanishi and Voldman is improper.

As discussed above, Nakanishi does not disclose testing the electrical connections, let alone how to use pads 3 in a testing operation. Accordingly, there is no disclosed need or desire for providing the diode of Voldman in the circuit of Nakanishi in the manner set forth by the Examiner, rendering the proposed modification without the requisite motivation/rationale ***from the prior art***.

Based on all the foregoing, it is submitted that claims 4 and 5 are patentable over Nakanishi in view of Voldman. Accordingly, it is respectfully requested that the rejection of claims 4 and 5 under 35 U.S.C. § 103 be withdrawn.

CONCLUSION

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication for which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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